REMARKS

This communication is being filed in response to the final Office Action having a mailing date of July 31, 2006. Applicants have placed all claims in condition for allowance.

The applicants thank the Examiner for the allowance of claims 17-20. In addition, the Examiner indicated that claims 3-6 and 8-10 are objected to and would be allowed.

Accordingly, the limitations of independent claim 1 have been placed into claim 3, and claim 1 has been canceled. Dependent claim 2 has been amended to depend from independent claim 3. Additionally, the limitations of independent claim 7 have been integrated into claim 8, and claim 7 has been canceled. In addition, claim 11 has been amended to place it in allowable form based on the instructions from the Examiner with respect to other claims in the case and in light of the art, so that claim 11 is clearly allowable. In this response, claims 2-13 and 17-20 are outstanding.

An earnest effort has made to place all claims in condition for allowance so the patent can be passed to issue. Applicants' attorney understands that this is a final Office Action. Accordingly, in order to facilitate entry of this amendment, all of the Examiner's suggestions have been adopted and all of the claims have been amended to be placed in a form which the Examiner will find allowable so that the case can be advanced to issue.

As applicants have stated, claim 11 has been amended to be allowable based on the prior art which has been made of record, and the distinctions recognized by the Examiner, so that further searching and further consideration is not necessary. In order to assist the Examiner in understanding the allowable subject matter of claim 11, the following remarks are provided.

Additional remarks with respect to claims 3-6, 8-10, and 17-20 will not be provided since these claims have already been indicated as allowable by the Examiner.

I. Discussion of non-limiting embodiments of the present invention as compared to the cited prior art

Claim 11 is patentable, as amended, over the cited reference, U.S. Patent No. 6,119,226 to Shiau et al., ("Shiau").

A. Disclosed embodiment(s) of the present invention allow address bits to determine which one of several memory devices is selected

Referring jointly to claim 11 and FIG. 2 in the present application, which shows one embodiment of the present invention covered by claim 11, there are disclosed several separate and independent memory devices, not just memory cells contained in the same memory device. Some are 4Mbit devices; others are 8Mbit devices. Paragraph [0019] of the present application provides a detailed description of FIG. 2. Such embodiments of the present invention indicate that more than one memory device may be placed on the circuit board, and each of these separate memory devices share a common address bus. Memory Controller 3 (*see* FIG. 1) drives the common address bus, and several of the bits in the address are used to determine which one of the separate memory devices the Memory Controller 3 is communicating with.

Paragraph [0023] discloses that each of the separate memory devices may include four ID pins, and the four ID pins of each separate memory device are asserted in a unique way. Paragraph [0024] describes an embodiment where the assertion on the four ID pins is such that each memory device has a sequential binary address. The first memory device has no ID pins asserted (providing for address 0000); the second memory device has its first ID pin asserted (providing for address 0001); the third memory device has its next ID pin asserted (providing for address 0010); and this pattern may be continued for up to 16 separate memory devices- all sharing the same address bus.

Paragraph [0026] discloses that in some embodiments, four of the address bits driven by the Memory Controller 3 (Bits A<24:21> for example) are compared to the four ID pins of each memory chip. If the memory chip determines that the four address bits, A<24:21>, match the signal level on its four ID pins, then the device will continue to process the communications from the Memory Controller 3, and the memory device may be written or read. On the contrary, if the memory chip determines that the four address bits, A<24:21>, do not match the signal level on its four ID pins, then the memory device resets its internal state machine and will not respond to the Memory Controller.

Paragraphs [0060] – [0069] describe this functionality in greater detail. As can be seen from the discussion above, which refers to claim 11, some embodiments of the present

invention include a plurality of separate memory devices on the same address bus, and bits coded into the address on the bus will be used to enable a single memory device while all other memory devices on the bus are disabled. The cited prior art does not contemplate this feature of multiple memory devices.

B. The cited prior art reference only teaches a single memory device

As cited by the Examiner, Shiau's invention will decode a memory address into either top-down or bottom-up protocol. Also, the Examiner points to Shiau's abstract, column 2, and Figure 1 for the proposition that Shiau discloses "a memory" with "other memories." The applicants acknowledge that Shiau teaches a memory array including "rows and columns of memory cells," but he applicants assert that Shiau's memory cells must all be contained in a single memory device containing a single row detector and a single address decoder and not in "other memories." Unlike claim 11 in the present application, Shiau has no possible way of allowing more than one memory device on his address bus.

C. A non-limiting example describing one difference between the present invention and the cited prior art

A non-limiting example, which refers to claim 11 of the present application, will now be described to help the Examiner appreciate the significant difference between Shiau and claim 11 of the present application. In the example, both claim 11 of the present application and the Shiau prior art attempt to place two separate memory devices on the same address bus. It will be shown that the Shiau invention is incapable of this operation.

If, for example, both inventions attempt to put two 4 Mbit memory devices on the same address bus (as in FIG. 2 of the present application), then each memory device can address 512 KBytes (2^19 = 524,288 bytes = 4,194,304 bits). The internal address range of each memory device is: A<31-0> = 0000 0000h to 0007 FFFFh. Notice that address bits A<31-19> are all zero.

In claim 11 of the present invention, address bits A<24-21>, for example, may be used to determine which of the two memory devices the memory controller is attempting to

communicate with. The memory controller may use these bits and this will be transparent to the internal architecture of each memory device's memory array. In such case, for example, the first memory device may have all of its ID pins tied to ground, and the second memory device may have three of its ID pins tied to ground and the fourth ID pin tied to board voltage. Then, the memory controller may communicate with the first memory device by setting upper address bits A<24-21> equal to 0000b, and the memory controller may communicate with the second memory device by setting upper address bits A<24-21> equal to 0001b. In this example, the memory controller will communicate with the first memory device if it sets the address bus to A<31-0> = 0000 0000h to 0007 FFFFh; and the memory controller will communicate with the second memory device if it sets the address bus to A<31-0> = 0020 0000h to 0027 FFFFh.

The Shiau invention discloses, teaches, or suggests no method of distinguishing between the two memory devices. If both devices are placed on the address bus, then both devices will attempt to communicate with the memory controller at the same time, and the system will not work. Accordingly, each claim that discloses "other memory devices" or a "one or more memory devices" and "matching the identification signals to a first set of addressing pins" is distinguishable over Shiau and therefore allowable.

II. Discussion of the claim rejections

A. Dependent claim 2

The applicant asserts that independent claim 2 is distinguishable over Shiau for reasons beyond the reason for allowance of claim 3. The LPC protocol, as "performed in the LPC decoding block" recited in claim 2 demands particular sequences of clock, address, data, and control signals. The Shiau invention does not disclose, teach or suggest the LPC protocol, and therefore, claim 2 is individually distinguishable over Shiau. Nevertheless, because the applicants have chosen to amend the independent claim from which claim 2 depends, the point is moot in this response.

B. Independent claim 11 and dependent claims 12-13

As described above in the examples of non-limiting embodiments, Shiau does not disclose, teach, or suggest a system whereby more than a single memory device can be placed on the address bus. More specifically, Shiau does not disclose, teach, or suggest using address bits that are available on the address bus to uniquely identify a specific memory device. Nevertheless, the Examiner has indicated a belief that Shiau's "rows and columns of memory cells" anticipates "a plurality of memory circuits" as recited in claim 11. Accordingly, the applicants have amended claim 11 to recite "one or more memory devices." This amendment, in light of the discussion above and the Examiner's instructions, now places claim 11 and its dependent claims in condition for allowance, and the applicants respectfully request this indication from the Examiner.

III. Conclusion

This amendment is made in order to reach agreement on the present claims and have the case advanced to allowance. Applicants may wish to file a continuation in which they pursue some subject matter more similar to the currently pending claims rather than to the allowed claims or incorporating some of the amendments which were included herein. Such claims, if presented, will be pursued in the continuation, and the present claims have been amended so as to clearly place all claims in condition for allowance.

Overall, the Shiau reference does not disclose, teach, or suggest what is recited in the independent claims. Thus, given the above remarks, it is respectfully submitted that the presently rejected independent claims are in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

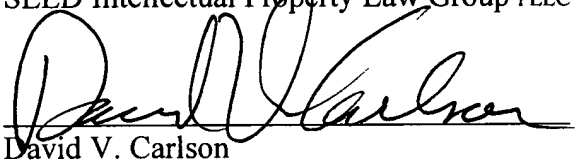
If the applicants' attorney, Mr. Carlson, has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact Mr. Carlson at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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